OIPE JC68 DEC 29 2000 PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 2207/9800	SERIAL NO. 09/708,722
	APPLICANT: JOURDAN et al	
	FILING DATE November 9, 2000	GROUP Not assigned

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	
BJO	5,381,533	Jan. 10, 1995	Peleg et al	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION	
					YES	NO

OTHER DOCUMENTS

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
BJO	Black et al, "The Block-Based Trace Cache", Proceedings of The 26th Int'l. Symposium on Computer Architecture, May 2-4, 1999, Atlanta, Georgia
BJO	Conte et al, "Optimization of Instruction Fetch Mechanisms for High Issue Rates", Proceedings of The 22nd Annual Int'l. Symposium on Computer Architecture, June 22-24, 1995, Santa Margherita Ligure, Italy
BJO	Dutta et al, "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors", Proceedings of The 28th Int'l. Symposium on Microarchitecture, Nov. 29-Dec. 1, 1995, Ann Arbor, Michigan
BJO	Friendly et al, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", Proceedings of The 30th Annual IEEE/ACM Int'l. Symposium on Microarchitecture, Dec.1-3, 1997, Research Triangle Park, North Carolina
BJO	Intrater et al, "Performance Evaluation of a Decoded Instruction Cache for Variable Instruction-Length Computers", Proceedings of The 19th Annual Int'l. Symposium on Computer Architecture, May 19-21, 1992, Gold Coast, Australia
BJO	Jacobson et al, "Path-Based Next Trace Prediction", Proceedings of The 30th Annual Int'l. Symposium on Microarchitecture, Dec. 1-3, 1997, Research Triangle Park, North Carolina
EXAMINER	DATE CONSIDERED 9/15/03

EXAMINER: Initial if citation is considered, whether or not citation is in conformance with M.P.E.P. 609, strike out citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
BJO	McFarling, Scott, "Combining Branch Predictors", June 1993, WRL Technical Note TN-36, Digital Western Research Laboratory, Palo Alto, California
BJO	Michaud et al, "Exploring Instruction-Fetch Bandwidth Requirement in Wide-Issue Superscalar Processors", Proceedings of The 1999 Int'l. Conference on Parallel Architectures and Compilation Techniques, Oct. 12-16, 1999, Newport Beach, California
BJO	Patel et al, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing", Proceedings of The 25th Annual Int'l. Symposium on Computer Architecture, June 27-July 1, 1998, Barcelona, Spain
BJO	Reinman et al, "A Scalable Front-End Architecture for Fast Instruction Delivery", Proceedings of The 26th Int'l. Symposium on Computer Architecture, May 2-4, 1999, Atlanta, Georgia
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BJO	Seznec et al, "Multiple-Block Ahead Branch Predictors", Proceedings of The 7th Int'l. Conference on Architectural Support for Programming Languages and Operating Systems, Oct. 1-4, 1996, Cambridge, United States
BJO	Yeh et al, "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache", Proceedings of The 7th Int'l. Conference on Supercomputing, July 1993

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